

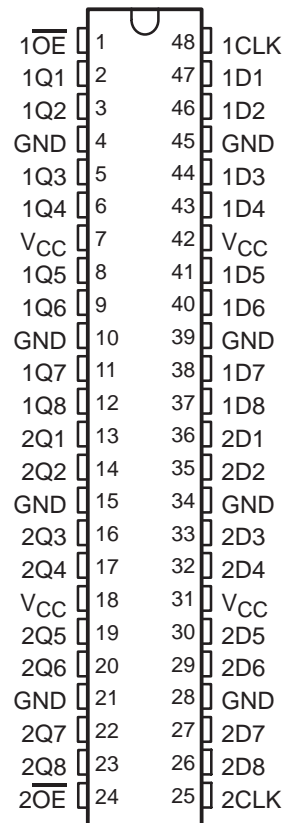
SN74LVC16374A

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS663D – MARCH 2001 – REVISED AUGUST 2003

- Member of the Texas Instruments Widebus™ Family
- Typical V_{OLP} (Output Ground Bounce) $<0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $>2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V V_{CC})
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74LVC16374ADL	LVC16374A
		Tape and reel	SN74LVC16374ADLR	
	TSSOP – DGG	Tape and reel	SN74LVC16374ADGGR	LVC16374A
	TVSOP – DGV	Tape and reel	SN74LVC16374ADGVR	LD374A
	VFBGA – GQL	Tape and reel	SN74LVC16374AGQLR	LD374A
VFBGA – ZQL (Pb-free)	SN74LVC16374AZQLR			

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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description/ordering information

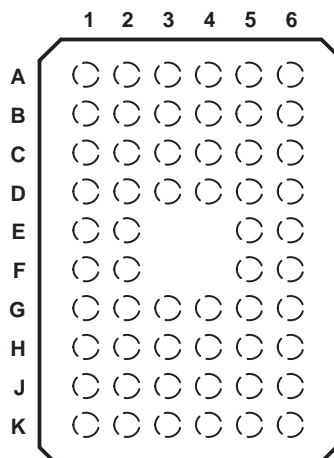
\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQL OR ZQL PACKAGE
(TOP VIEW)



terminal assignments

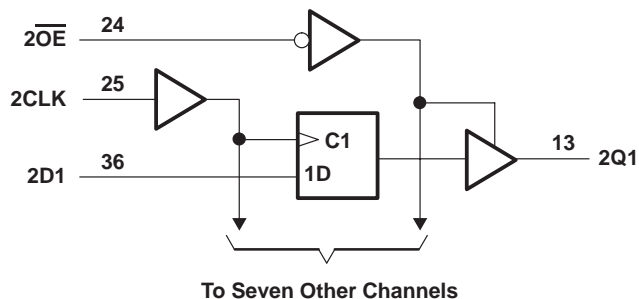
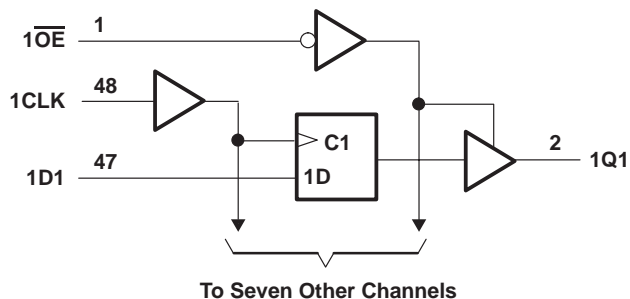
	1	2	3	4	5	6
A	$\overline{1OE}$	NC	NC	NC	NC	1CLK
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	$\overline{2OE}$	NC	NC	NC	NC	2CLK

NC – No internal connection

FUNCTION TABLE
(each flip-flop)

	INPUTS			OUTPUT Q
	\overline{OE}	CLK	D	
L	L	↑	H	H
L	L	↑	L	L
L	L	H or L	X	Q_0
H	H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, and DL packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The value of V_{CC} is provided in the recommended operating conditions table.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	3.6	V
	Data retention only	1.5		
V_{IH} High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	1.7		
	$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL} Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		V
	$V_{CC} = 2.3$ V to 2.7 V	0.7		
	$V_{CC} = 2.7$ V to 3.6 V	0.8		
V_I Input voltage		0	5.5	V
V_O Output voltage	High or low state	0	V_{CC}	V
	3-state	0	5.5	
I_{OH} High-level output current	$V_{CC} = 1.65$ V	–4		mA
	$V_{CC} = 2.3$ V	–8		
	$V_{CC} = 2.7$ V	–12		
	$V_{CC} = 3$ V	–24		
I_{OL} Low-level output current	$V_{CC} = 1.65$ V	4		mA
	$V_{CC} = 2.3$ V	8		
	$V_{CC} = 2.7$ V	12		
	$V_{CC} = 3$ V	24		
$\Delta t/\Delta v$ Input transition rise or fall rate			10	ns/V
T_A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V
	I _{OH} = -4 mA	1.65 V	1.2			
	I _{OH} = -8 mA	2.3 V	1.7			
	I _{OH} = -12 mA	2.7 V	2.2			
	I _{OH} = -24 mA	3 V	2.4			
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 0 to 5.5 V	3.6 V			±5	μA
I _{off}	V _I or V _O = 5.5 V	0			±10	μA
I _{OZ}	V _O = 0 to 5.5 V	3.6 V			±10	μA
I _{CC}	V _I = V _{CC} or GND	3.6 V	I _O = 0		20	μA
	3.6 V ≤ V _I ≤ 5.5 V‡				20	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V			5	pF
C _o	V _O = V _{CC} or GND	3.3 V			6.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	150		150		150		150		MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2.4		1.6		1.9		1.9		ns
t _h	Hold time, data after CLK↑	0.8		1		1.1		1.9		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		150		MHz
t _{pd}	CLK	Q	1	6.5	1	4.3	1	4.9	1.5	4.5	ns
t _{en}	\overline{OE}	Q	1	6.7	1	4.7	1	5.3	1.5	4.6	ns
t _{dis}	\overline{OE}	Q	1	10.7	1	5	1	6.1	1.5	5.5	ns
t _{sk(o)}									1		ns



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WITH 3-STATE OUTPUTS

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operating characteristics, $T_A = 25^\circ\text{C}$

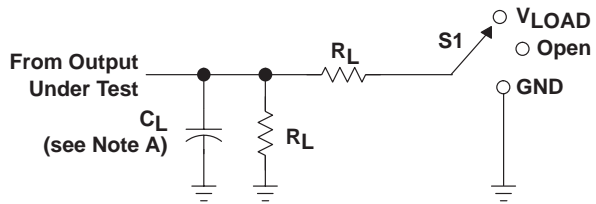
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz 47	52	58	pF
		Outputs disabled	21	23	24	

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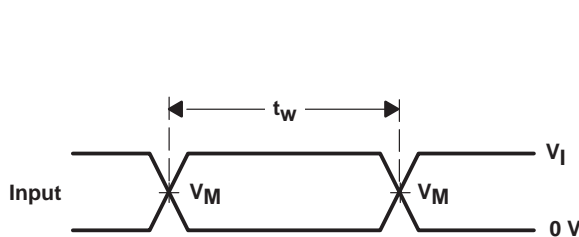
PARAMETER MEASUREMENT INFORMATION



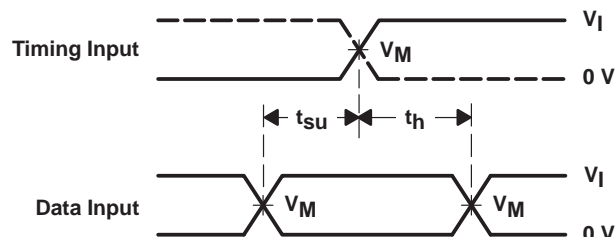
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	VLOAD
t_{PHZ}/t_{PZH}	GND

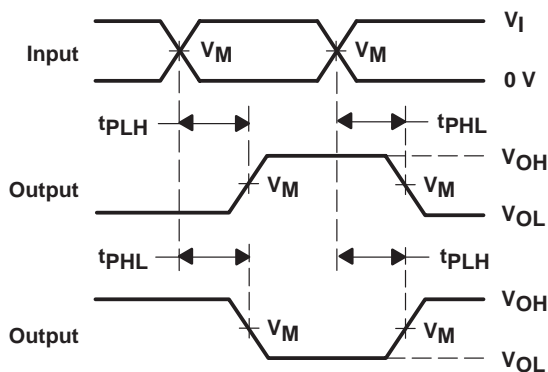
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	V_{CC}	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



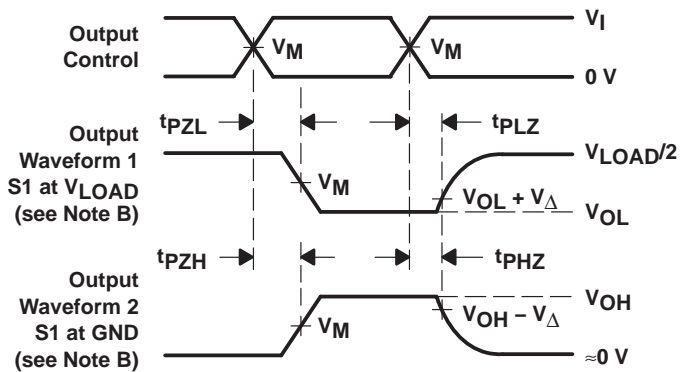
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

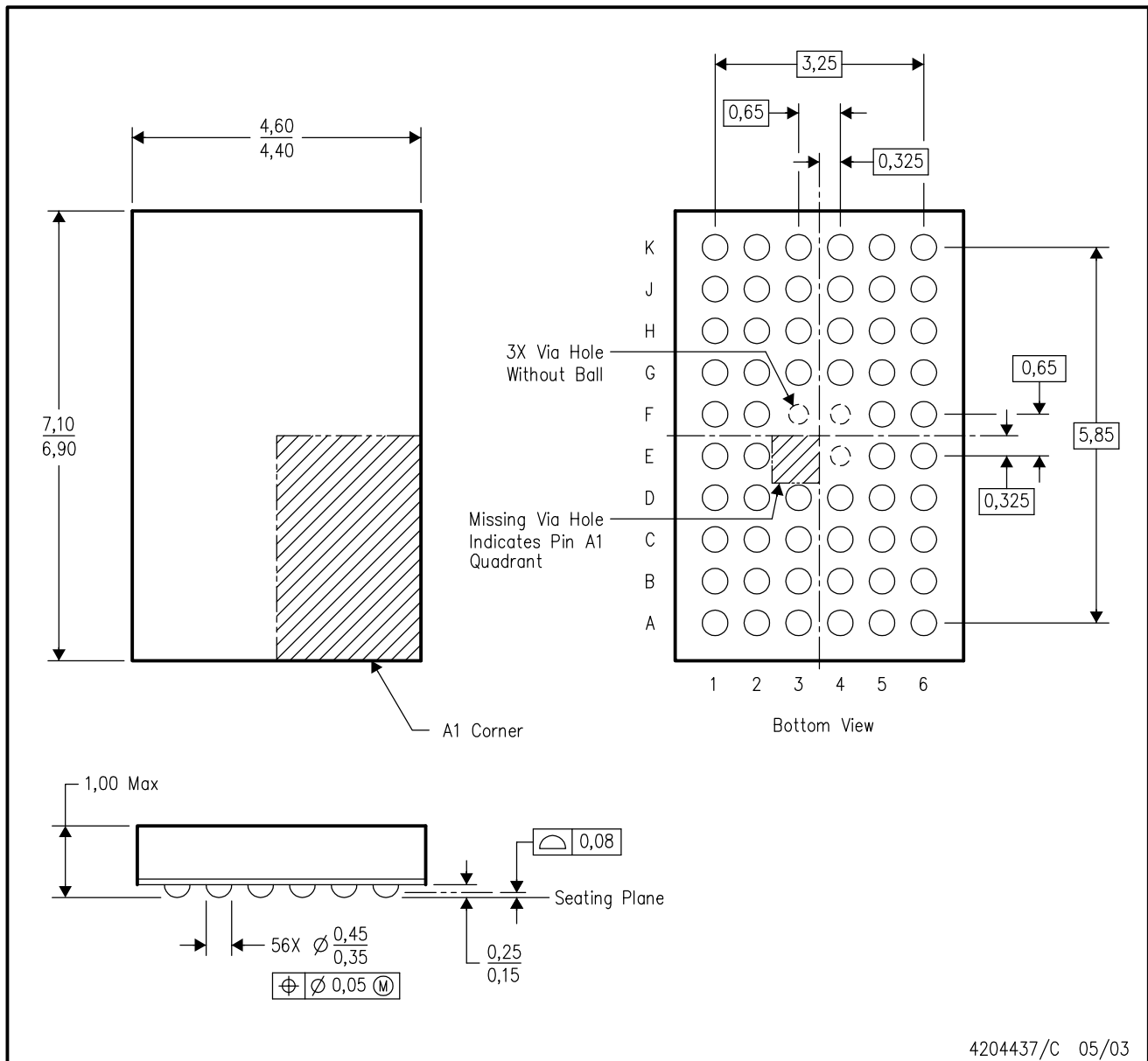
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY

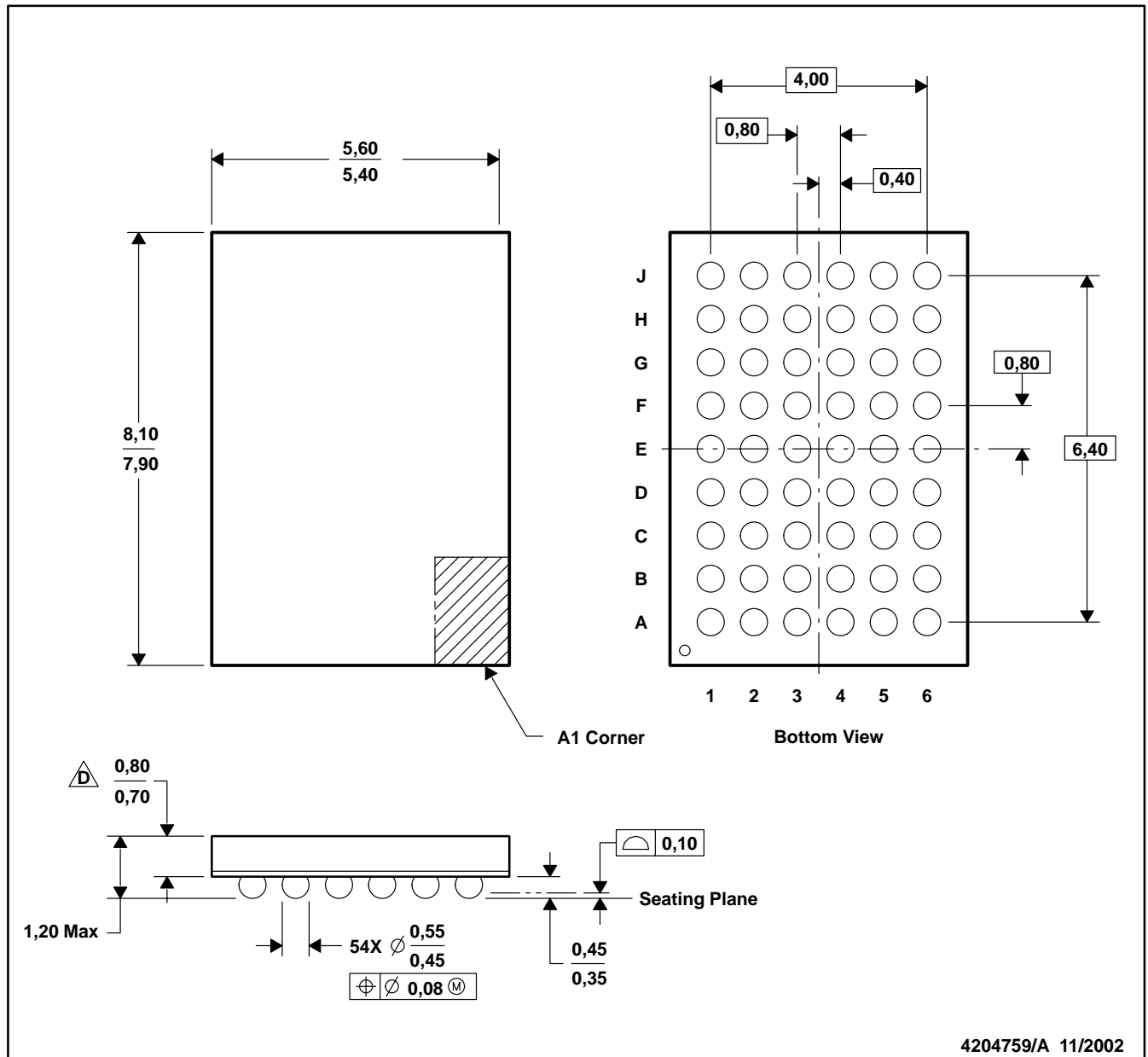


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration.
 - D. Falls within JEDEC MO-225 variation BA.
 - E. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

GRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



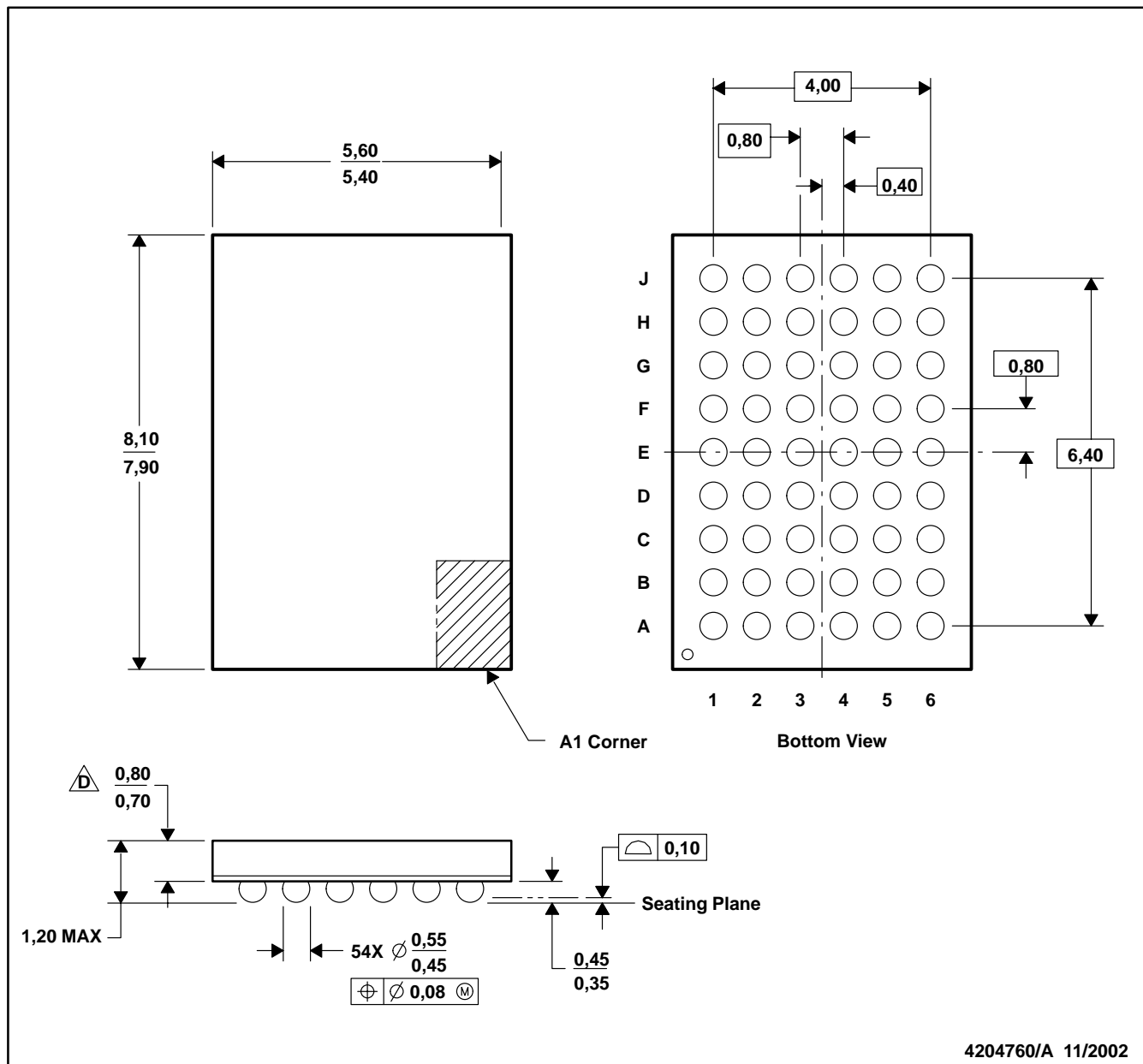
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar Junior™ BGA configuration.
 D. Falls within JEDEC MO-205 variation DD, except for body thickness.
 E. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 420760) for lead-free.

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ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar Junior™ BGA configuration.
 D. Falls within JEDEC MO-205 variation DD, except for body thickness.
 E. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

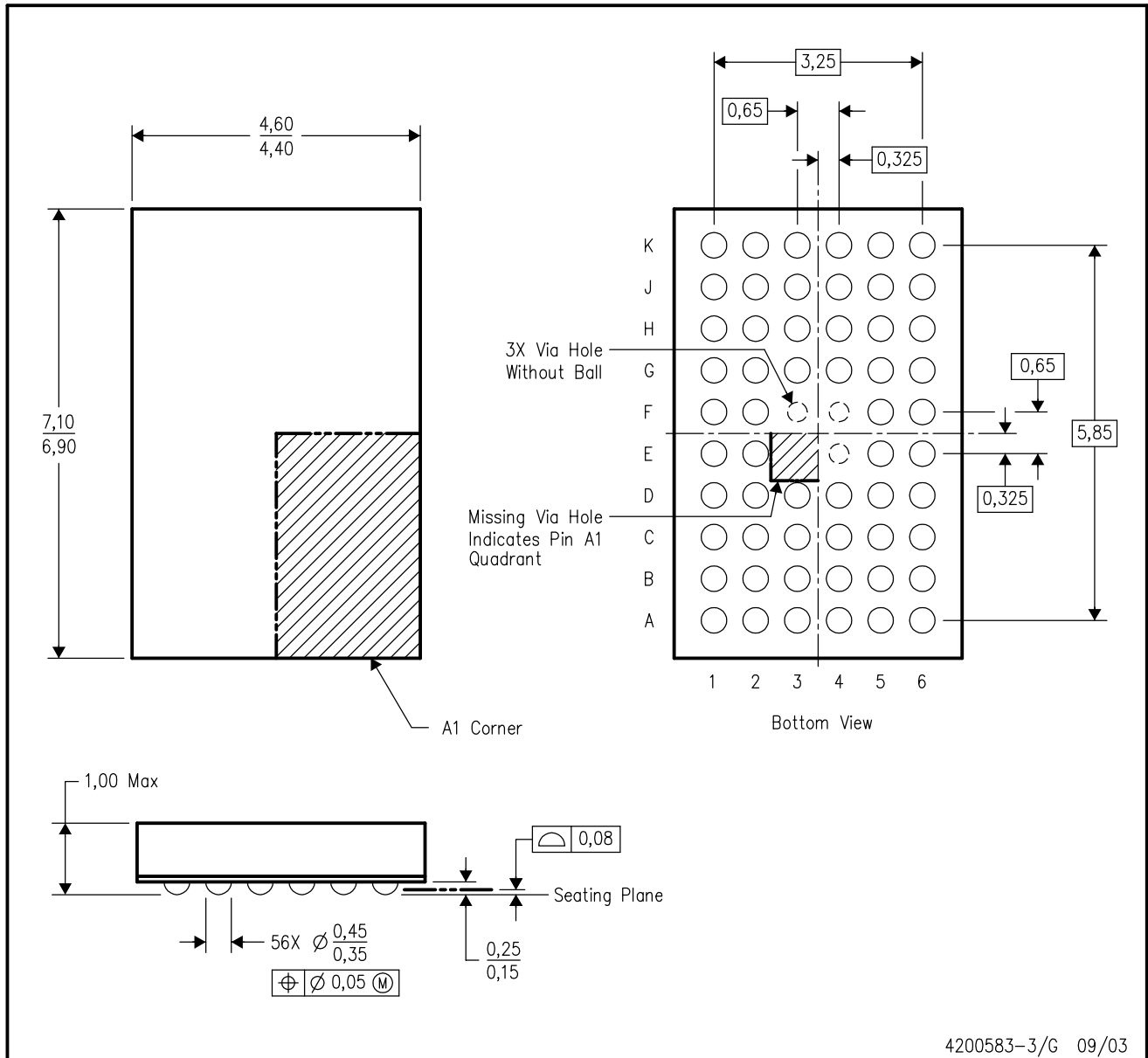
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



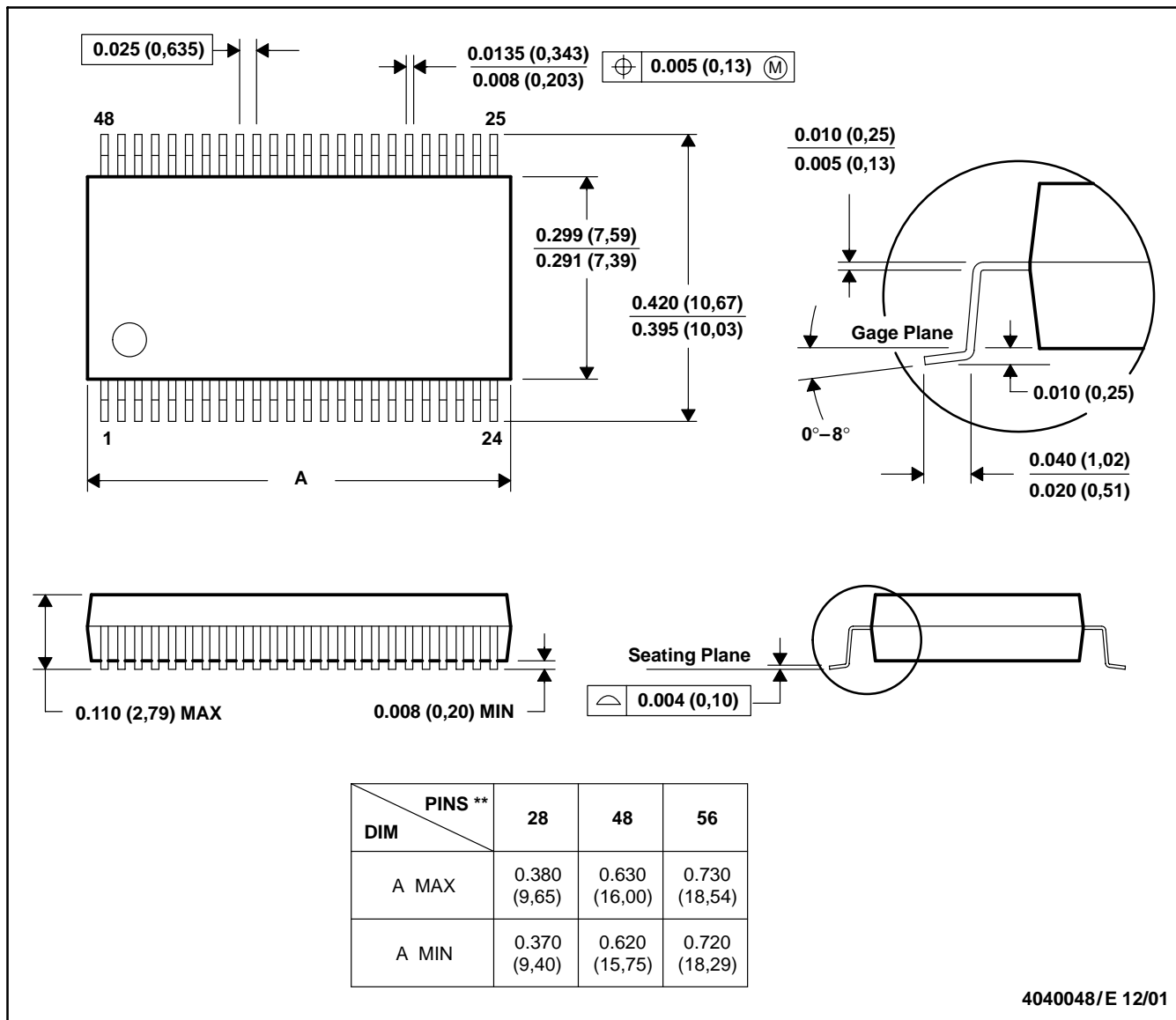
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. MicroStar Junior™ BGA configuration.
 - D. Falls within JEDEC MO-225 variation BA.
 - E. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

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DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

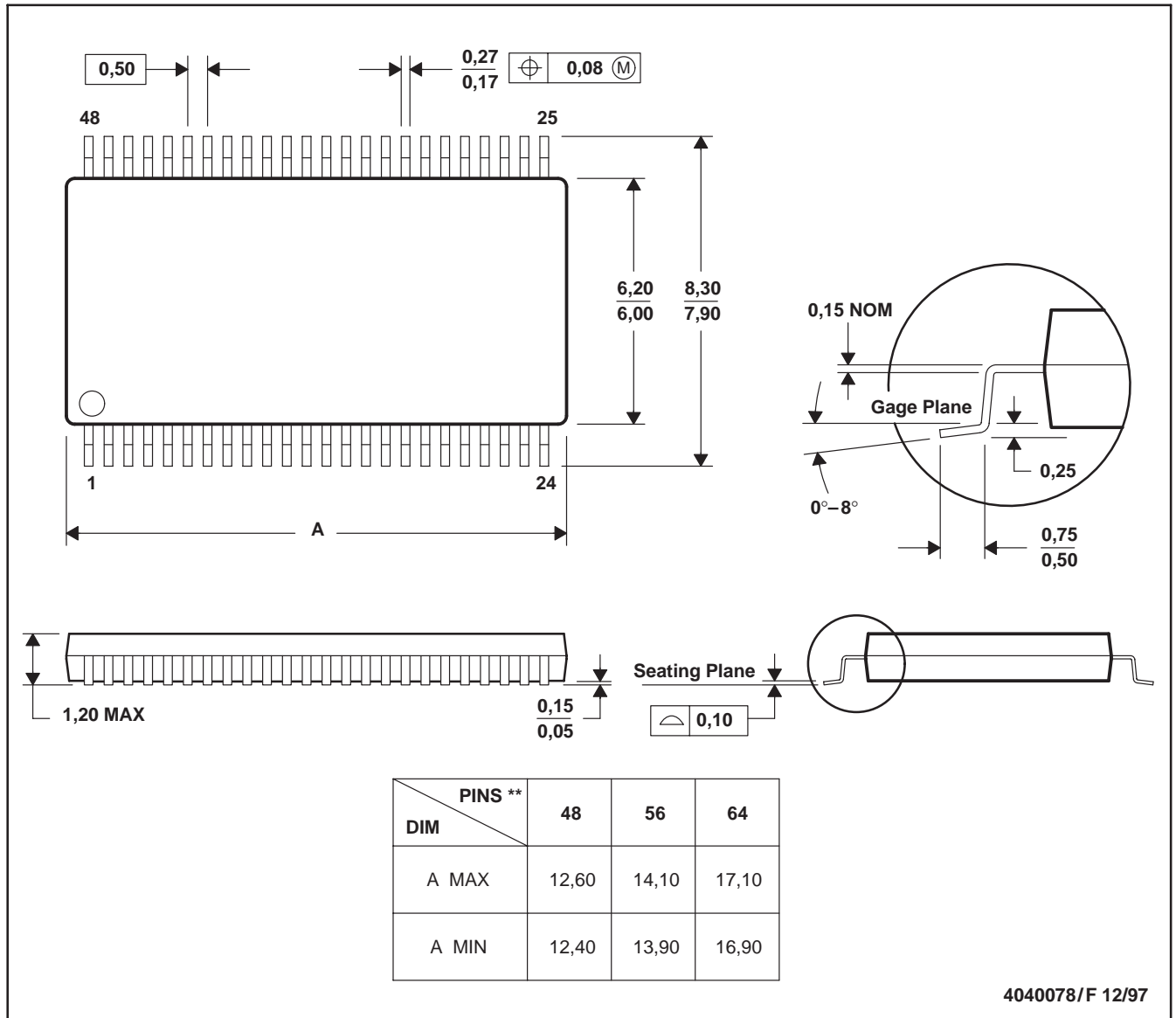


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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